ABSTRACT OF THE DISCLOSURE

A method of manufacturing a non-volatile memory array having vertical field effect transistors is revealed. First, a semiconductor substrate having multiple trenches is provided, and then dopants are implanted into the semiconductor substrate to form first doping regions and second doping regions respectively serving as source and drain bit lines at different heights. Secondly, a gate dielectric including at least one nitride film, e.g., an oxide/nitride/oxide (ONO) layer, is formed onto the surface of the semiconductor substrate, and polysilicon plugs serving as gate electrodes are filled up the multiple trenches afterward. After that, a polysilicon layer and a tungsten silicide (WiSix) layer are sequentially deposited followed by masking and etching processes to form parallel polycide lines serving as word lines, and then an oxide layer is deposited therebetween and planarized for isolation.